IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Wolrich, et al.	Art Unit	: 2187
Serial No.	: 10/780,330	Examiner	: Thammavong, Prasith
Filed	: February 17, 2004		
Title	: MEMORY MAPPING IN A PROCESSOR HAVING MULTIPLE PROGRAMMABLE UNITS		

REPLY BRIEF

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This Reply Brief is respectfully submitted in response to the Examiner's Answer mailed October 15, 2010

Status of claims

Claims 36-43 are pending in the case, stand rejected, and are being appealed.

Claims 1-35 and 44-45 are cancelled.

Grounds of rejection to be reviewed on appeal

Whether claims 36-43 were properly rejected under 35 U.S.C. s. 103(a) over Tremblay (U.S. Pat. 6,212,604) in view of Sharma (U.S. Pat. 6,055,605).

Argument

In the interest of brevity, arguments set forth in the Appeal Brief will not be repeated in this document. Nonetheless, these arguments are incorporated herein.

Claim 36 recites "mapping addresses in a single address space to resources within a set of multiple programmable units integrated within a processor" where "the single address space" includes "addresses for different ones of the resources in different ones of the multiple programmable units" and where "there is a one-to-one correspondence between respective addresses in the single address space and respective resources within the multiple programmable units."

The "Examiner's Response" of the "Examiner's Answer" relies on Tremblay's (U.S. 6,212,604) "use of an offset" to provide the recited 1:1 correspondence. While Attorney for Applicant agrees that in Tremblay, processors P1 and P2 add an offset to a specified register location within a register file (see col. 5, lines 47-62), Attorney for Applicant disagrees that the offset somehow can be equated with the recited subject matter.

For example, as correctly noted by the Examiner, Tremblay provides an example where P1 has an offset of 0 and P2 has an offset of 128. Thus, an instruction in the shared instruction cache to access some register location *x* when executed by P1 would result in an access to 0+*x* in P1's register file. An instruction specifying register *x* when executed by P2 would result in an access to 128+*x* in P2's register file.

One specified register address, 'x'. Two different locations accessed depending on which processor executes the instruction.

This is simply not a 1:1 correspondence between an address and a resource.

In short, the presence of the offset does not alter the analysis presented in the Appeal Brief. That is, offset or not, one specified register in Tremblay identifies two register locations: one in P1 and one in P2.

Conclusion

In view of the foregoing, favorable reconsideration and withdrawal of the rejections is respectfully requested. If there are any questions regarding the present application, the Examiner and/or Board is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

November 4, 2010
Date

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